AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A method of synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting a first edge of said data signal and a position of said first edge;

(B) determining if said position of said first edge is within a zone;

(C) if said first edge is not within said zone, adjusting said clock signal towards said position of said first edge;

(D) detecting a second edge of said data signal and a position of said second edge;

(E) determining a first value indicating ~~a~~ said position of said second edge;

(F) adding said first value to a second value to generate a third value, wherein said second value indicates a position of a third edge of said data signal; and

(G) adjusting said clock signal based on the result of ~~step (F)~~ said third value.

2. (CURRENTLY AMENDED) The method of claim 1, wherein step (E) further comprises:

comparing said third value to a predetermined value and ~~adjust~~ adjusting said clock signal only if said third value is greater than said predetermined value.

3. (CURRENTLY AMENDED) The method of claim 2, wherein step (B) further comprises:

determining if said third value is within a predetermined zone and adjusting said clock signal only if said third value is not within said predetermined zone.

4. (ORIGINAL) The method of claim 3, wherein step (B) further comprises:

comparing said third value to said predetermined zone.

5. (ORIGINAL) The method of claim 1, wherein step (E) further comprises selecting a number of clock phases based upon said third value.

6. (ORIGINAL) The method of claim 1, wherein step (F) further comprises:

adjusting said third value in response to said second value when adding said first value and said second value would cause an overflow or underflow.

7. (PREVIOUSLY PRESENTED) The method of claim 1, wherein step (E) further comprises:

incrementing or decrementing said first value.

8. (ORIGINAL) The method of claim 1, wherein step (F) further comprises:

storing said first value; and

storing said second value.

9. (CURRENTLY AMENDED) The method according to claim 1, wherein step (E) further comprises:

determining a high or low bandwidth in response to steps (A)-(D).

10. (CURRENTLY AMENDED) The method according to claim 1, wherein step (E) further comprises:

determining a plurality of ~~a~~ phase offset magnitudes in response to steps (A)-(D).

11. (ORIGINAL) The method according to claim 1, wherein step (E) further comprises:

determining a magnitude of said third value.

12. (CURRENTLY AMENDED) A method of synchronizing a clock signal to a data signal, comprising the steps of:

(A) upon power-up, performing said synchronization of said clock signal and said data signal with a high bandwidth system;

(B) after a predetermined amount of time, performing said synchronization of said clock signal and said data signal with a low bandwidth system; and

(C) adding a first value to a second value to produce a third value, wherein said second value represents a position of a second edge of said data signal.

13. (CURRENTLY AMENDED) An apparatus for synchronization of a clock signal to a data signal, comprising:

a detector configured to synchronize said clock signal and said data signal with a high bandwidth system, wherein said detector is configured after a predetermined amount of time to perform said synchronization of said clock signal and said data signal with a low bandwidth system; and

wherein the detector comprises an accumulator that adds a first value to a second value to produce a third value, wherein said second value represents a position of a second edge of said data signal.

14. (CANCELED)

15. (PREVIOUSLY PRESENTED) The apparatus of claim 13, wherein the detector is further configured to compare said third value to a predetermined value and adjust said clock signal only if said third value is greater than said predetermined value.

16. (CURRENTLY AMENDED) The apparatus of claim 13, wherein the detector is further configured to determine if said first value is within a predetermined zone and to adjust said clock signal only if said first value is not within said predetermined zone.

17. (PREVIOUSLY PRESENTED) The apparatus of claim 13, wherein the detector further comprises a register configured to store said second value, a register configured to store said first value, and an adder configured to add said first value and said second value.

18. (CURRENTLY AMENDED) The apparatus of claim 13, wherein said detector further comprises:

a comparator configured to compare said third value to said predetermined value~~; and~~

~~a look ahead circuit configured to generate an enable signal in response to overflow or underflow condition~~.

19. (CURRENTLY AMENDED) The apparatus of claim 18, wherein said detector further comprises an increment/decrement logic circuit configured to adjust said third value in response to said second value and ~~said~~ an enable signal.

20. (PREVIOUSLY PRESENTED) The apparatus of claim 13, wherein said clock signal comprises a plurality of phases and said

detector is configured to select one of said plurality of phases as a system clock.